FIG. 1

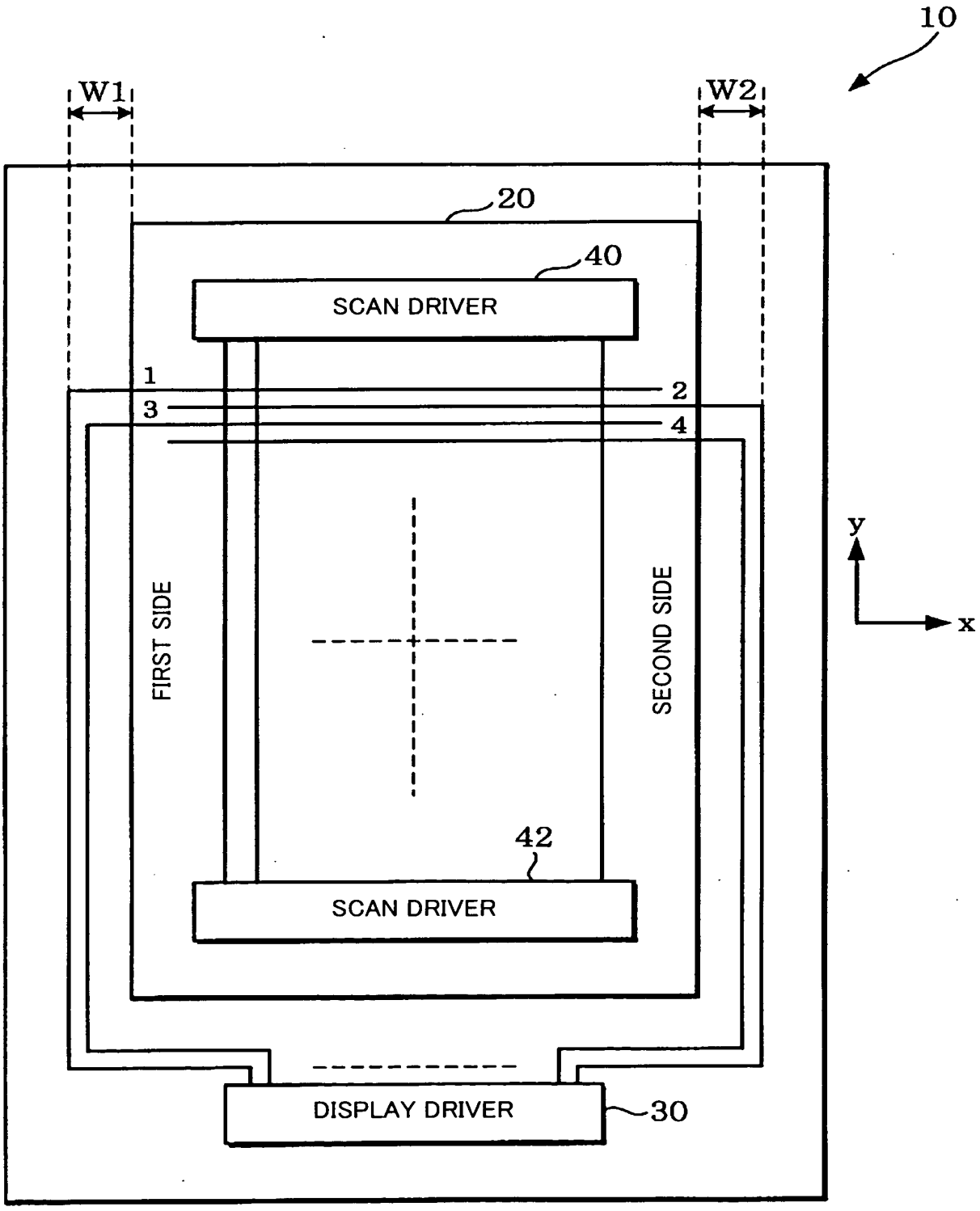

10
W1
W2
20
40
SCAN DRIVER
1
2
3
4
FIRST SIDE
SECOND SIDE
y
x
42
SCAN DRIVER
DISPLAY DRIVER
30

FIG. 2

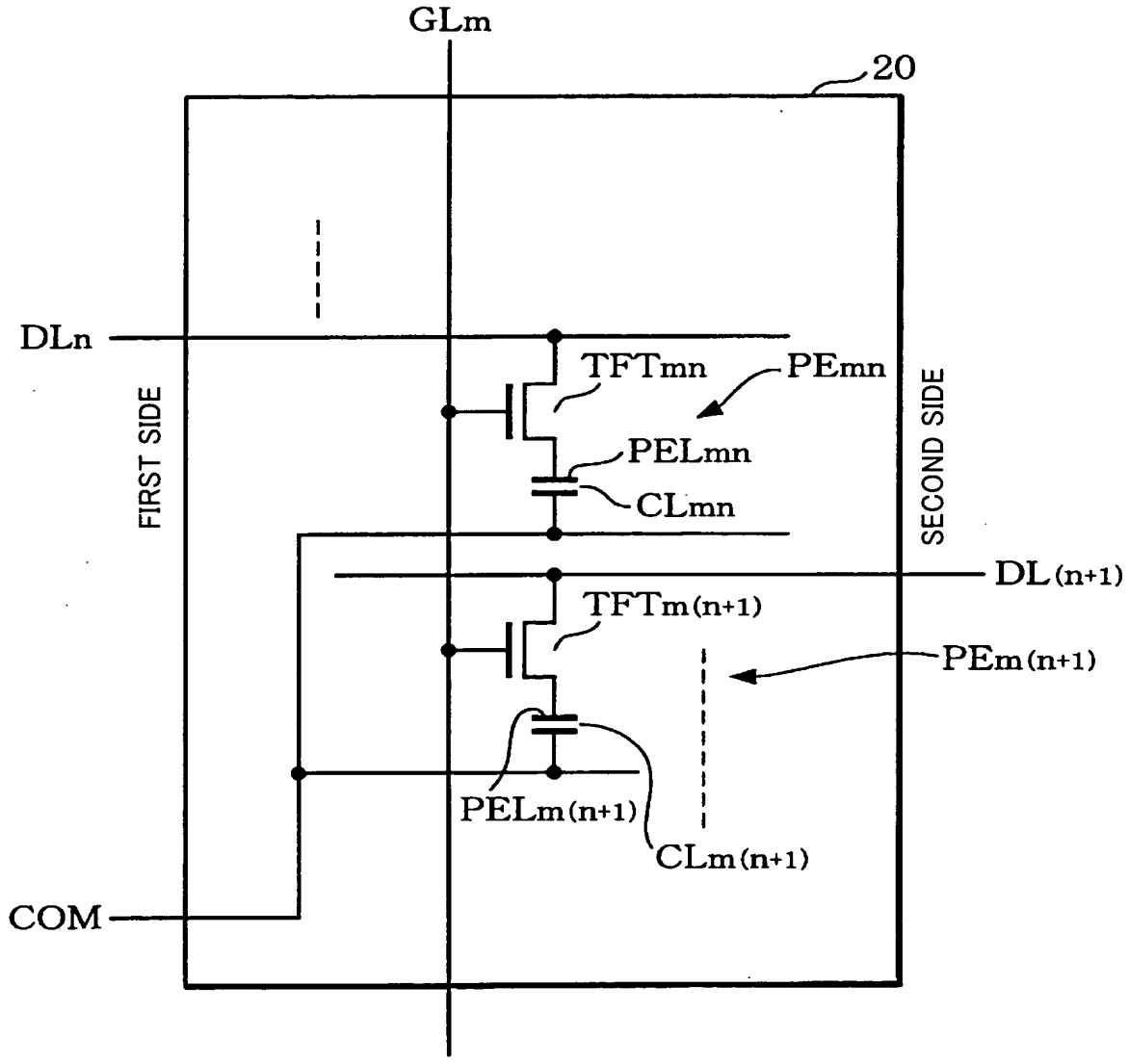

GLm
20
DLn
TFTmn
PEmn
PELmn
CLmn
FIRST SIDE
SECOND SIDE
DL(n+1)
TFTm(n+1)
PEm(n+1)
PELm(n+1)
CLm(n+1)
COM

FIG. 3

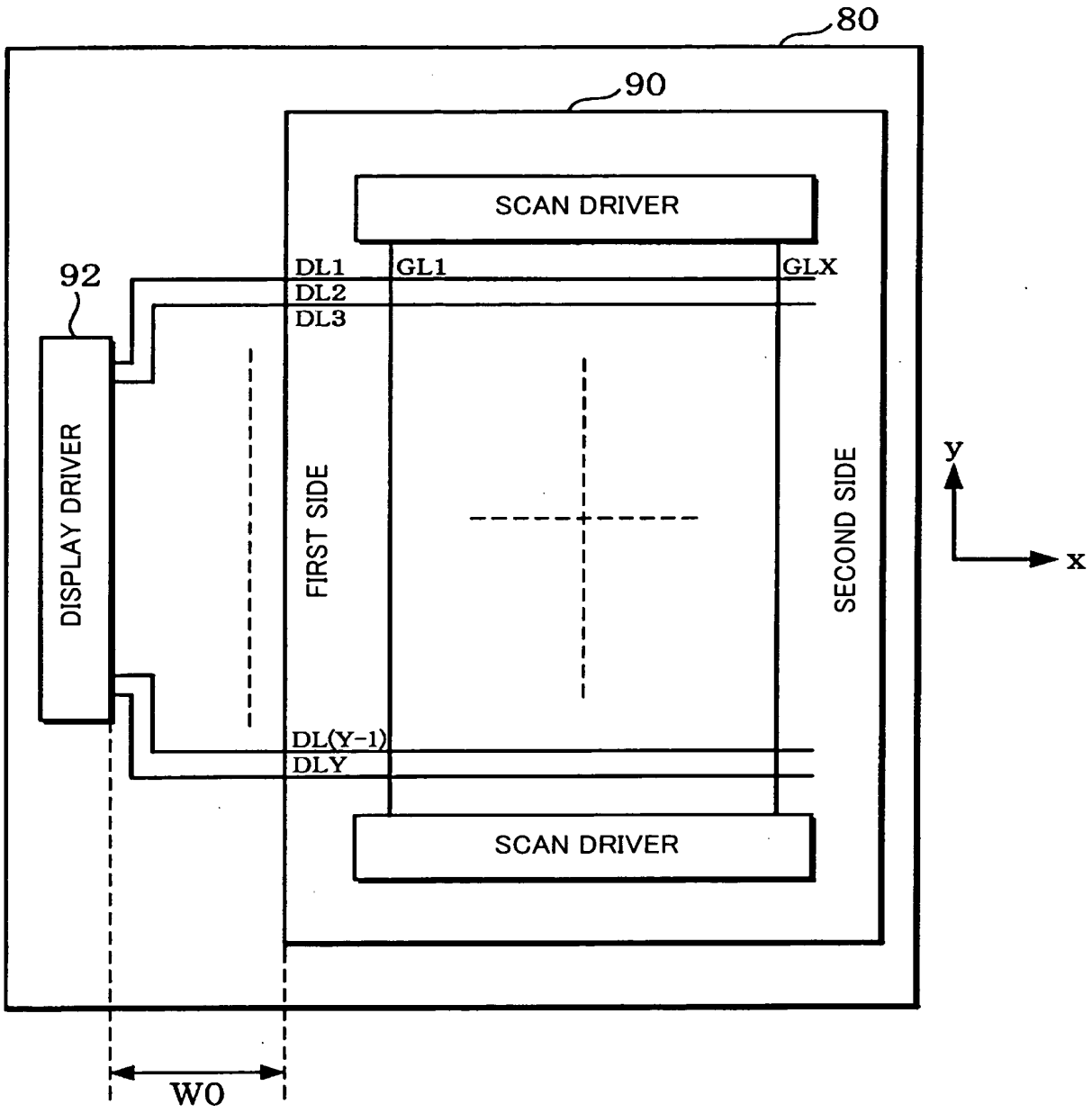

80
90
SCAN DRIVER
92
DL1
GL1
GLX
DL2
DL3
DISPLAY DRIVER
FIRST SIDE
SECOND SIDE
y
x
DL(Y-1)
DLY
SCAN DRIVER
W0

FIG. 4

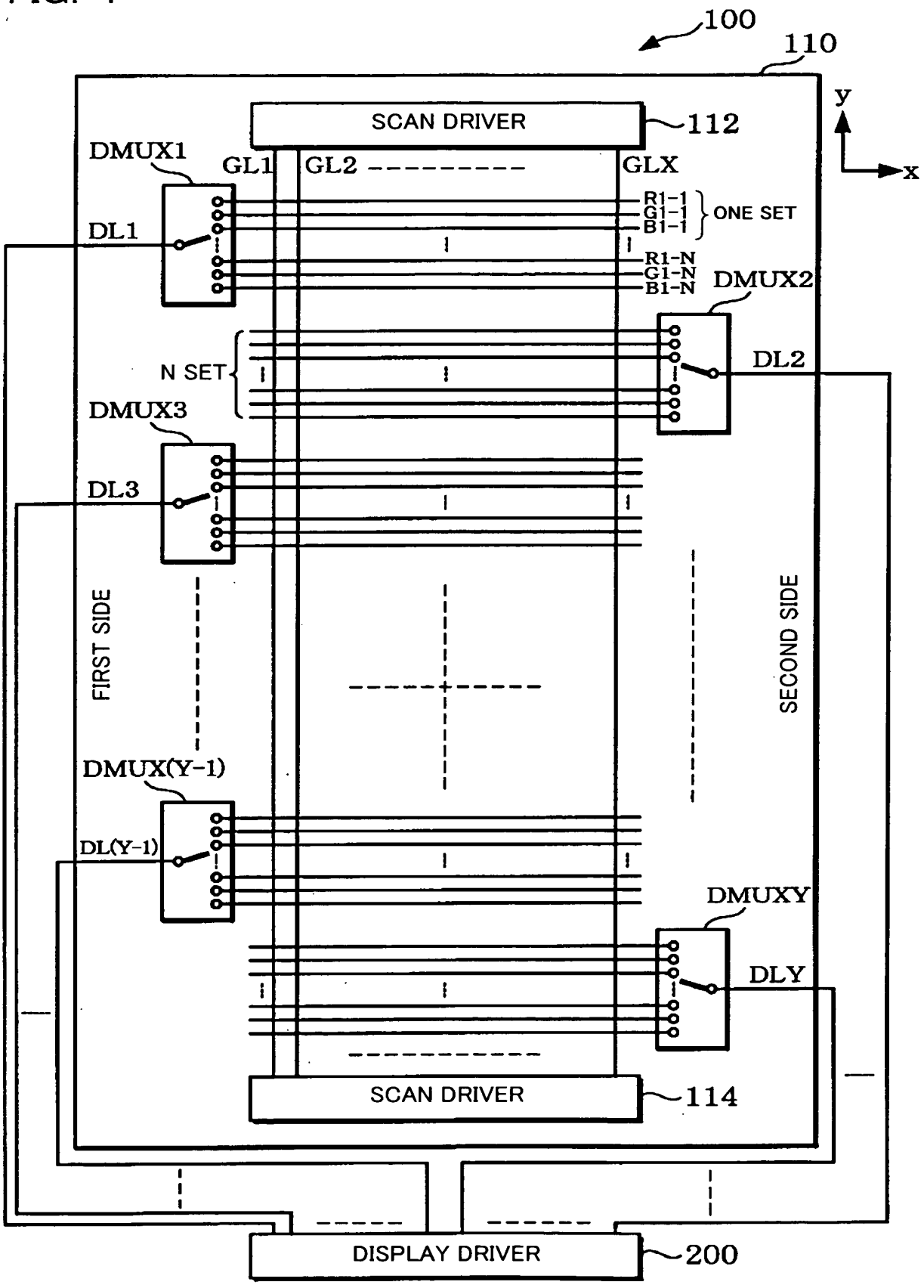

100
110
SCAN DRIVER
112
y
x
DMUX1
GL1
GL2
GLX
R1-1
G1-1
B1-1
ONE SET
DL1
R1-N
G1-N
B1-N
DMUX2
N SET
DL2
DMUX3
DL3
FIRST SIDE
SECOND SIDE
DMUX(Y-1)
DL(Y-1)
DMUXY
DLY
SCAN DRIVER
114
DISPLAY DRIVER
200

FIG. 5

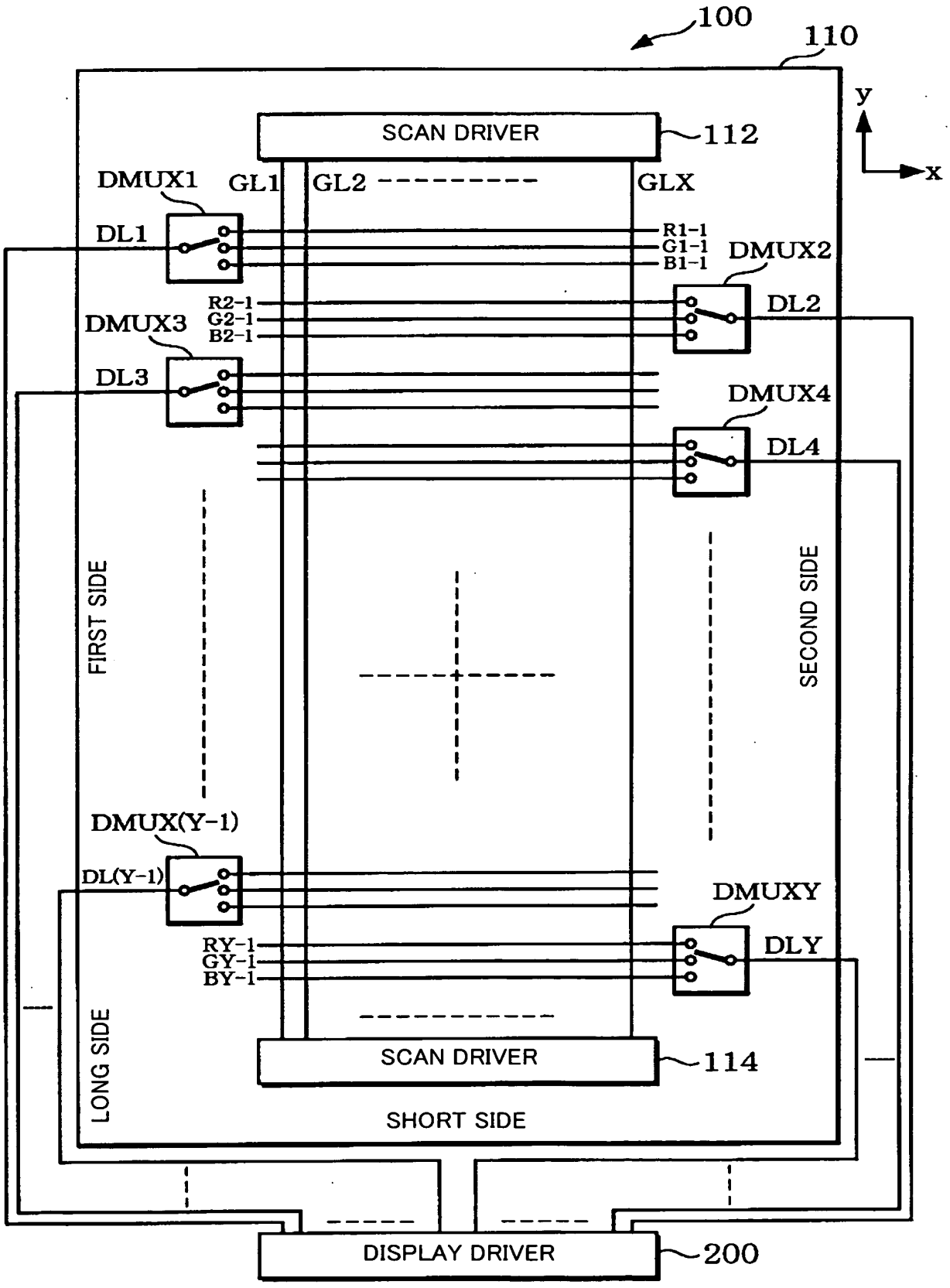

100
110
y
x
SCAN DRIVER
112
DMUX1
GL1
GL2
GLX
DL1
R1-1
G1-1
B1-1
DMUX2
DL2
R2-1
G2-1
B2-1
DMUX3
DL3
DMUX4
DL4
FIRST SIDE
SECOND SIDE
DMUX(Y-1)
DL(Y-1)
DMUXY
DLY
RY-1
GY-1
BY-1
LONG SIDE
SCAN DRIVER
114
SHORT SIDE
DISPLAY DRIVER
200

FIG. 6

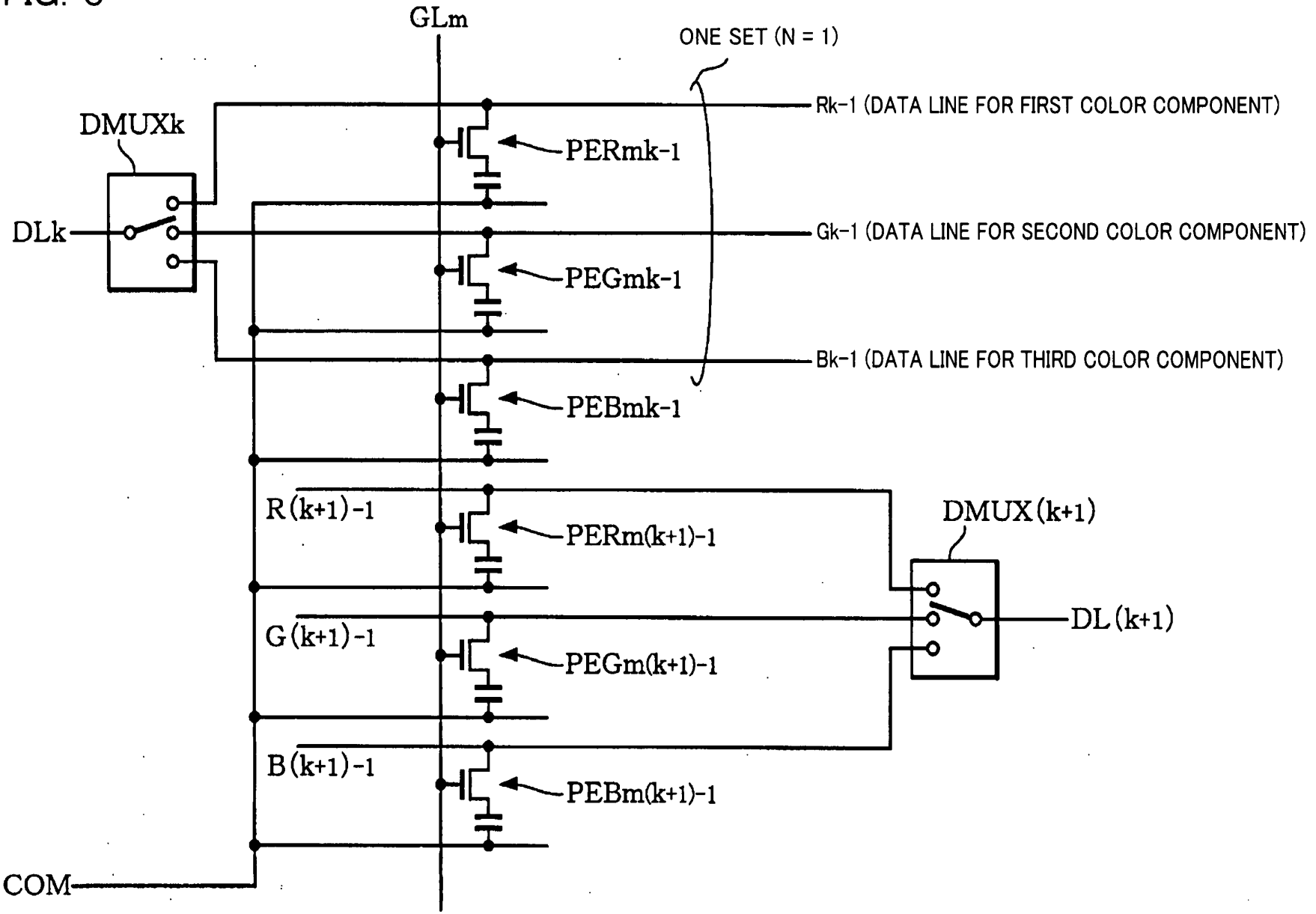

GLm
ONE SET (N = 1)
Rk-1 (DATA LINE FOR FIRST COLOR COMPONENT)
DMUXk
PERmk-1
DLk
Gk-1 (DATA LINE FOR SECOND COLOR COMPONENT)
PEGmk-1
Bk-1 (DATA LINE FOR THIRD COLOR COMPONENT)
PEBmk-1
R(k+1)-1
PERm(k+1)-1
DMUX(k+1)
G(k+1)-1
PEGm(k+1)-1
DL(k+1)
B(k+1)-1
PEBm(k+1)-1
COM

FIG. 7A

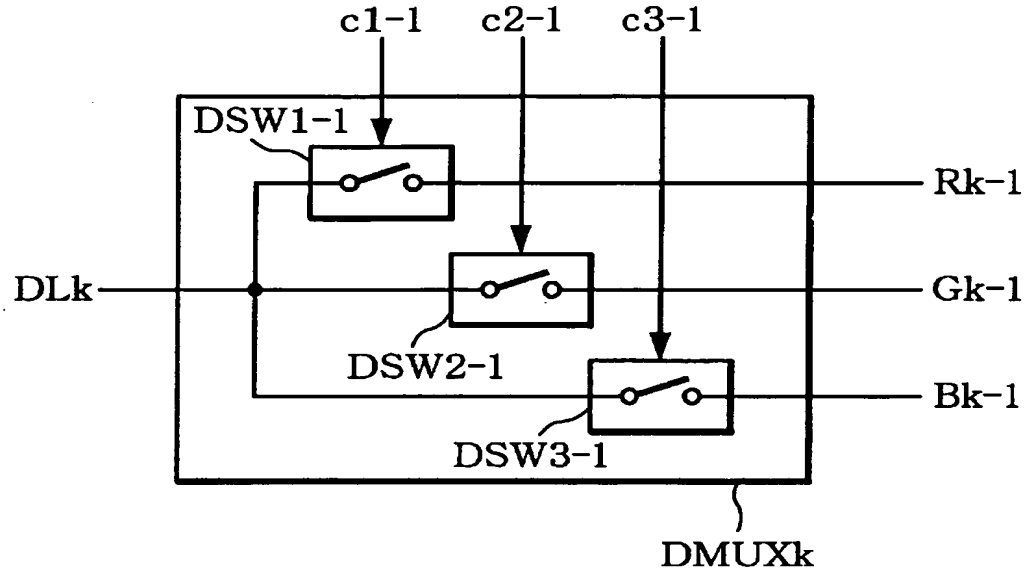

c1-1
c2-1
c3-1
DSW1-1
Rk-1
DLk
Gk-1
DSW2-1
Bk-1
DSW3-1
DMUXk

FIG. 7B

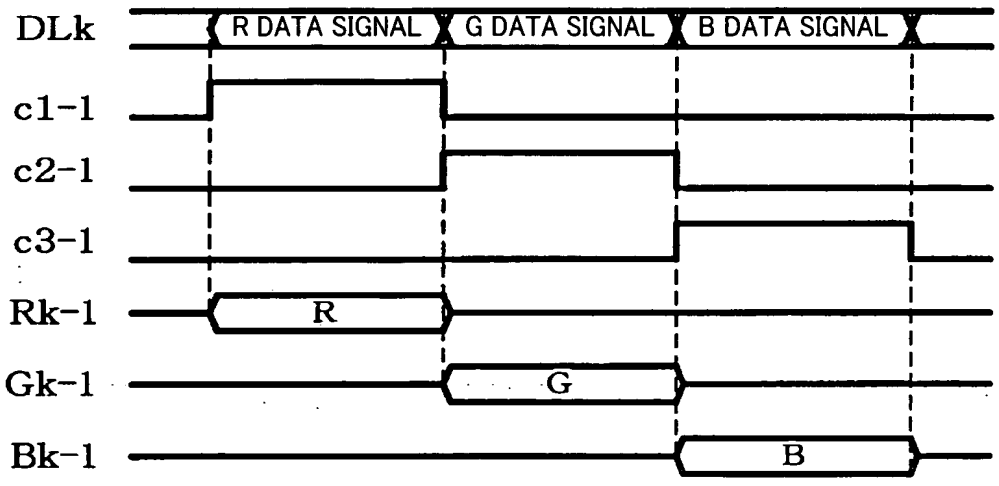

DLk
R DATA SIGNAL
G DATA SIGNAL
B DATA SIGNAL
c1-1
c2-1
c3-1
Rk-1
R
Gk-1
G
Bk-1
B

FIG. 8

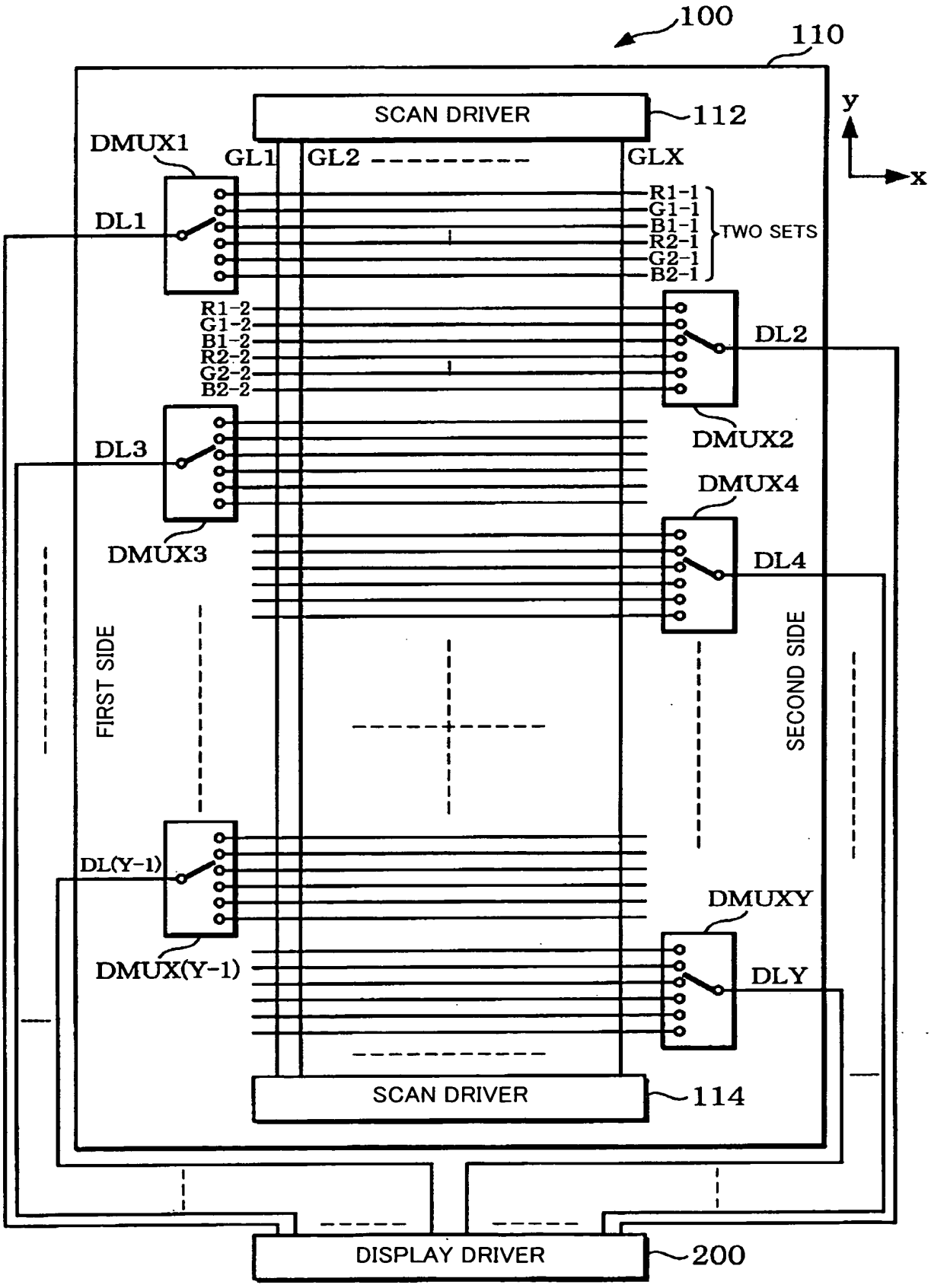

100
110
SCAN DRIVER
112
y
x
DMUX1
GL1
GL2
GLX
R1-1
G1-1
B1-1
R2-1
G2-1
B2-1
TWO SETS
DL1
R1-2
G1-2
B1-2
R2-2
G2-2
B2-2
DL2
DMUX2
DL3
DMUX4
DMUX3
DL4
FIRST SIDE
SECOND SIDE
DL(Y-1)
DMUXY
DMUX(Y-1)
DLY
SCAN DRIVER
114
DISPLAY DRIVER
200

FIG. 9A

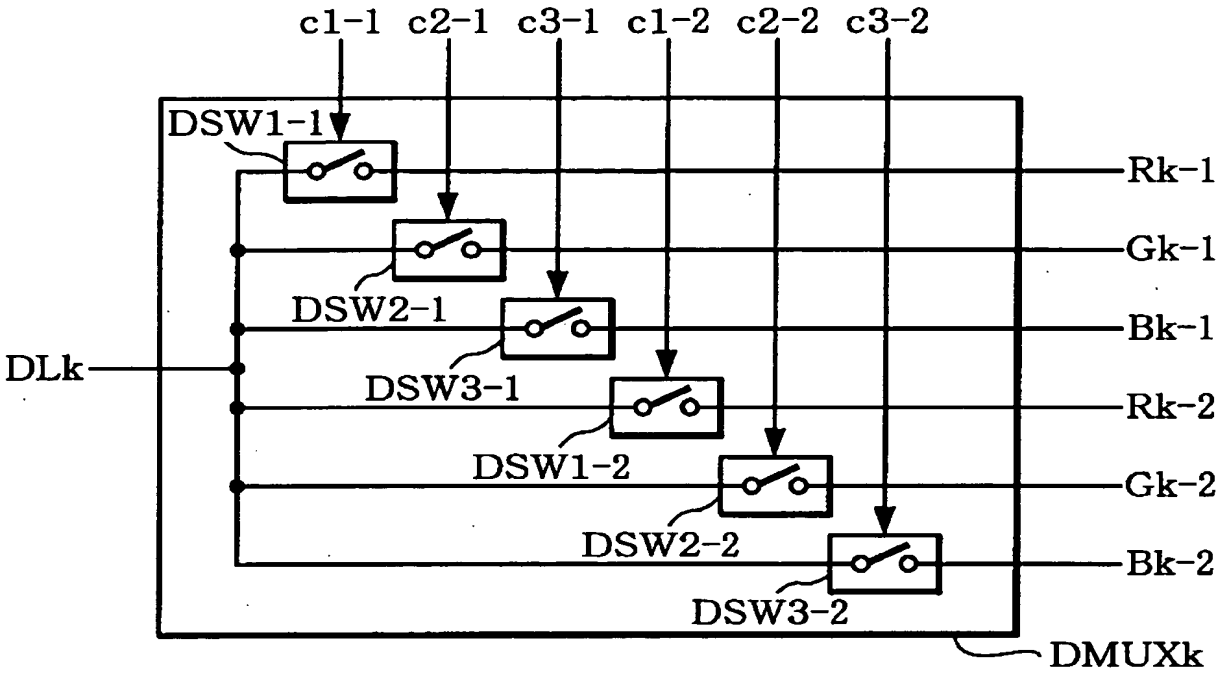

c1-1
c2-1
c3-1
c1-2
c2-2
c3-2
DSW1-1
DSW2-1
DSW3-1
DSW1-2
DSW2-2
DSW3-2
DLk
Rk-1
Gk-1
Bk-1
Rk-2
Gk-2
Bk-2
DMUXk

FIG. 9B

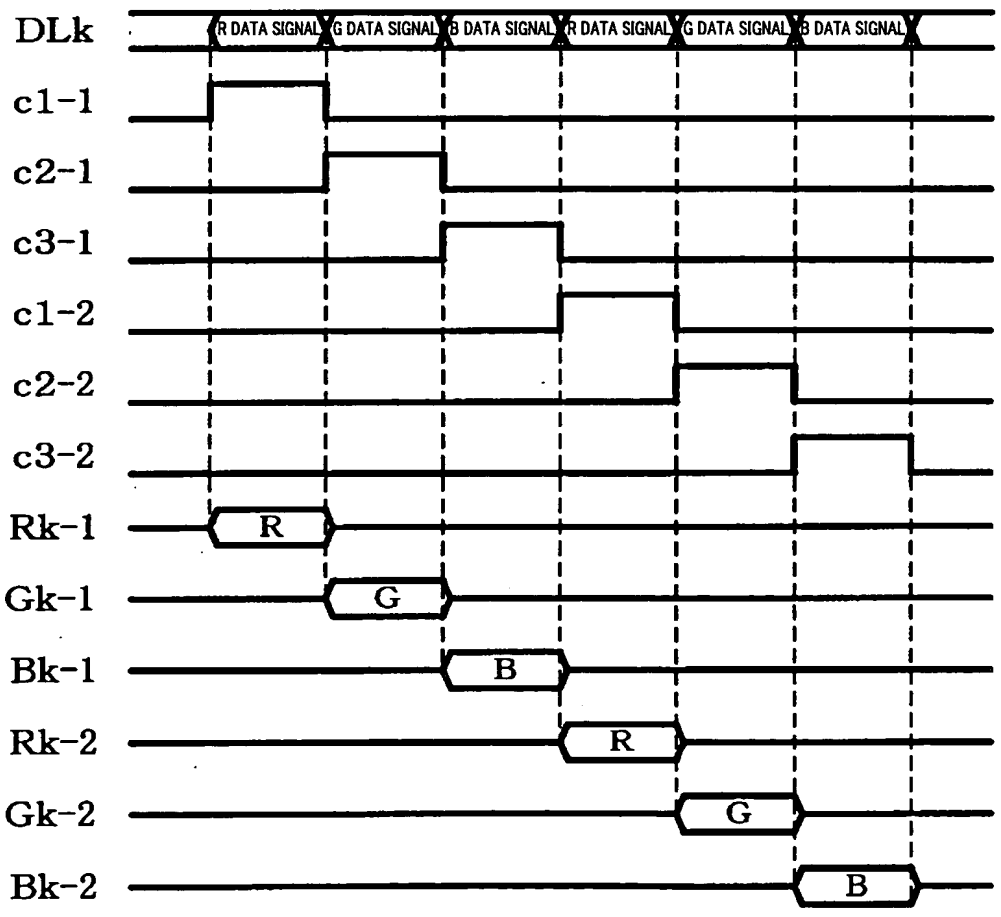

DLk
R DATA SIGNAL
G DATA SIGNAL
B DATA SIGNAL
R DATA SIGNAL
G DATA SIGNAL
B DATA SIGNAL
c1-1
c2-1
c3-1
c1-2
c2-2
c3-2
Rk-1
R
Gk-1
G
Bk-1
B
Rk-2
R
Gk-2
G
Bk-2
B

FIG. 10

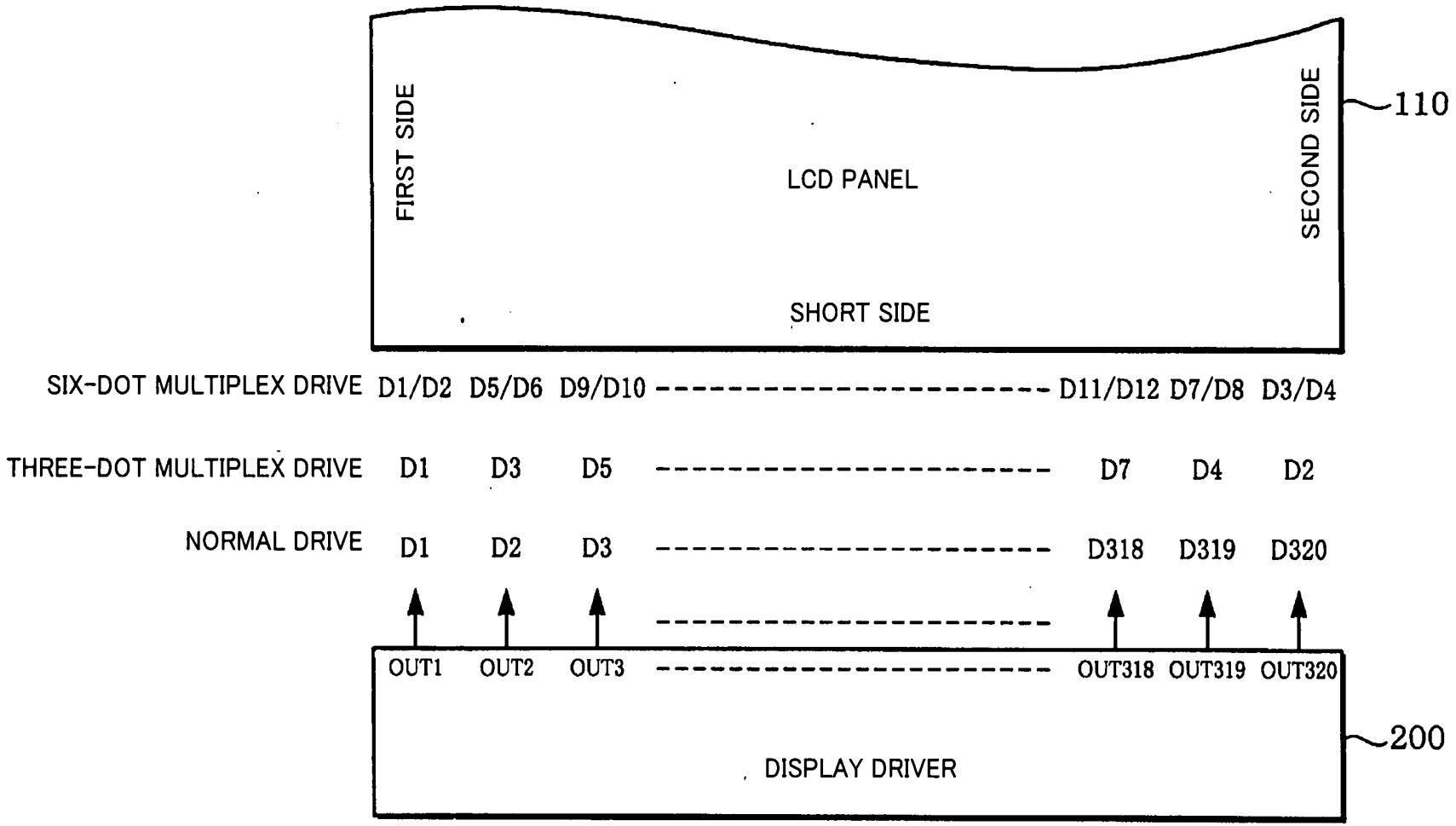

FIRST SIDE
LCD PANEL
SECOND SIDE
110
SHORT SIDE
SIX-DOT MULTIPLEX DRIVE
D1/D2 D5/D6 D9/D10 ---------- D11/D12 D7/D8 D3/D4
THREE-DOT MULTIPLEX DRIVE
D1 D3 D5 ---------- D7 D4 D2
NORMAL DRIVE
D1 D2 D3 ---------- D318 D319 D320
OUT1 OUT2 OUT3 ---------- OUT318 OUT319 OUT320
DISPLAY DRIVER
200

FIG. 11

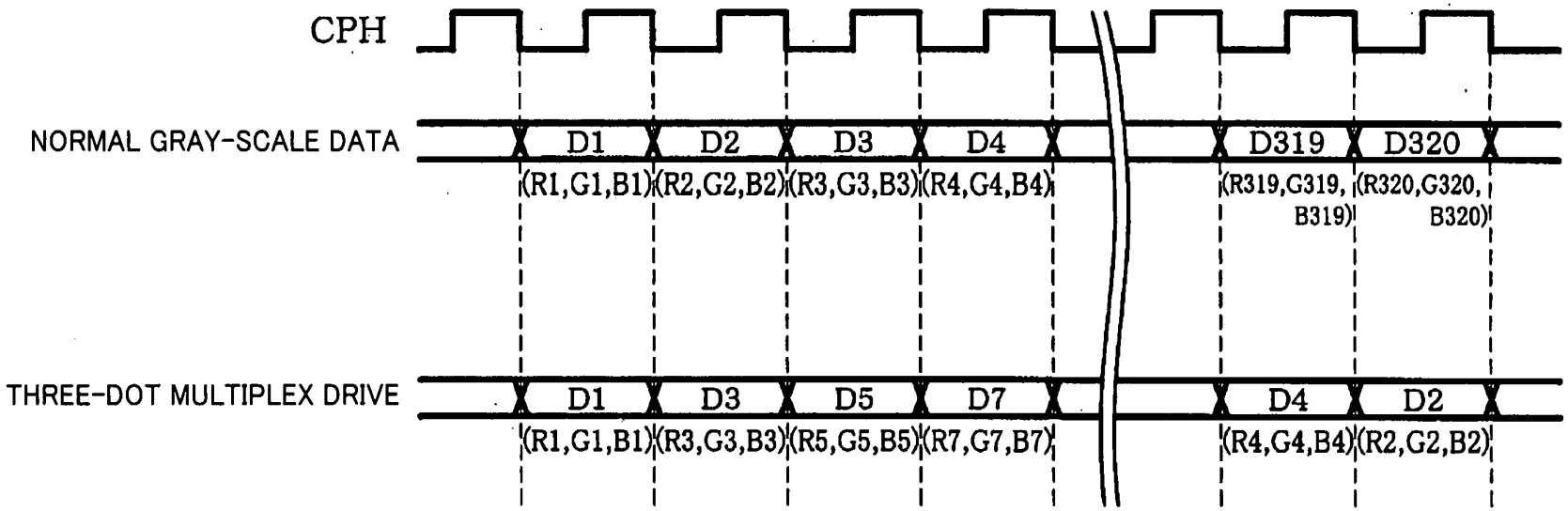

CPH
NORMAL GRAY-SCALE DATA
D1
D2
D3
D4
D319
D320
(R1,G1,B1)
(R2,G2,B2)
(R3,G3,B3)
(R4,G4,B4)
(R319,G319,B319)
(R320,G320,B320)
THREE-DOT MULTIPLEX DRIVE
D1
D3
D5
D7
D4
D2
(R1,G1,B1)
(R3,G3,B3)
(R5,G5,B5)
(R7,G7,B7)
(R4,G4,B4)
(R2,G2,B2)

FIG. 12

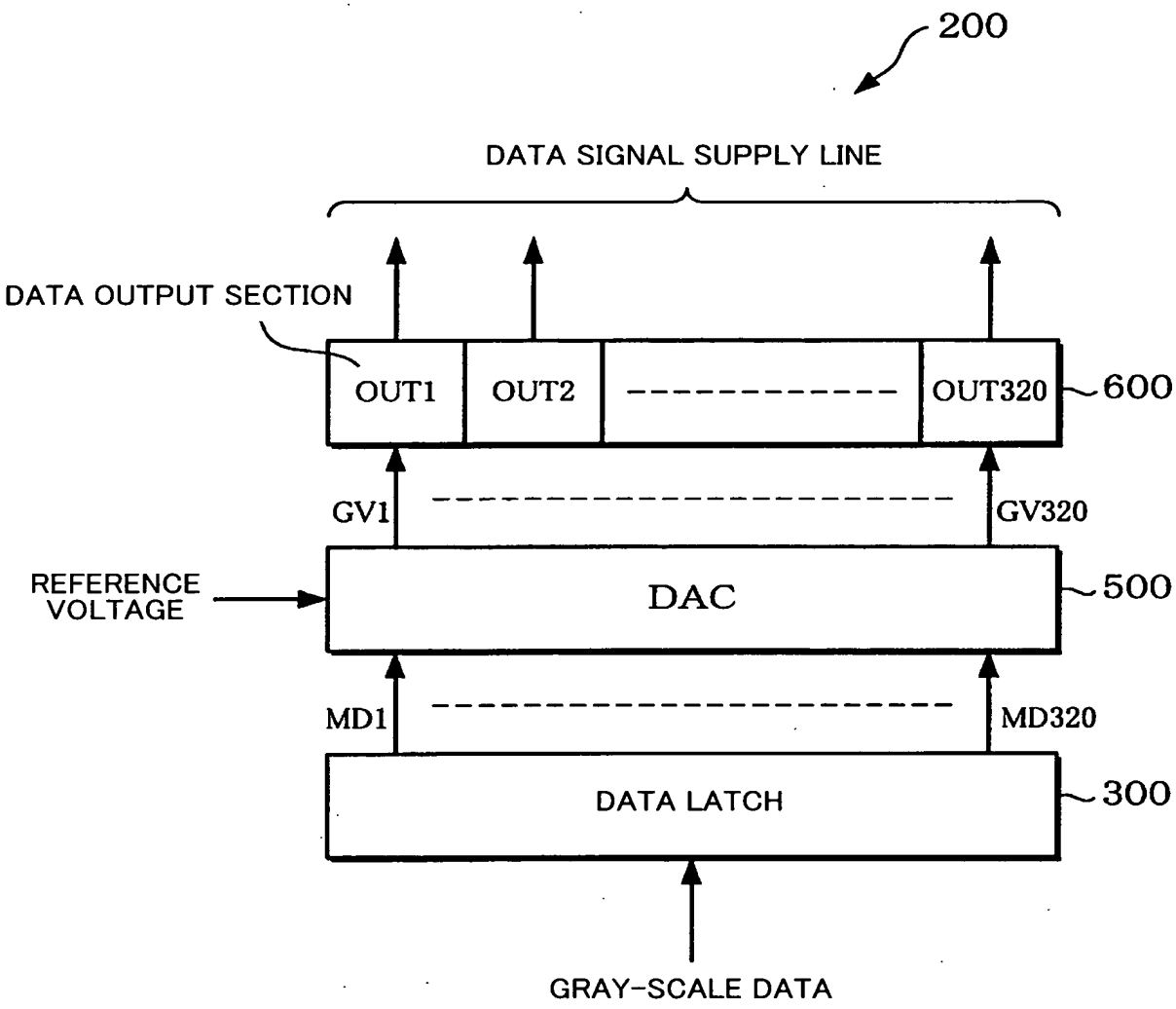

200
DATA SIGNAL SUPPLY LINE
DATA OUTPUT SECTION
OUT1
OUT2
OUT320
600
GV1
GV320
REFERENCE VOLTAGE
DAC
500
MD1
MD320
DATA LATCH
300
GRAY-SCALE DATA

FIG. 13

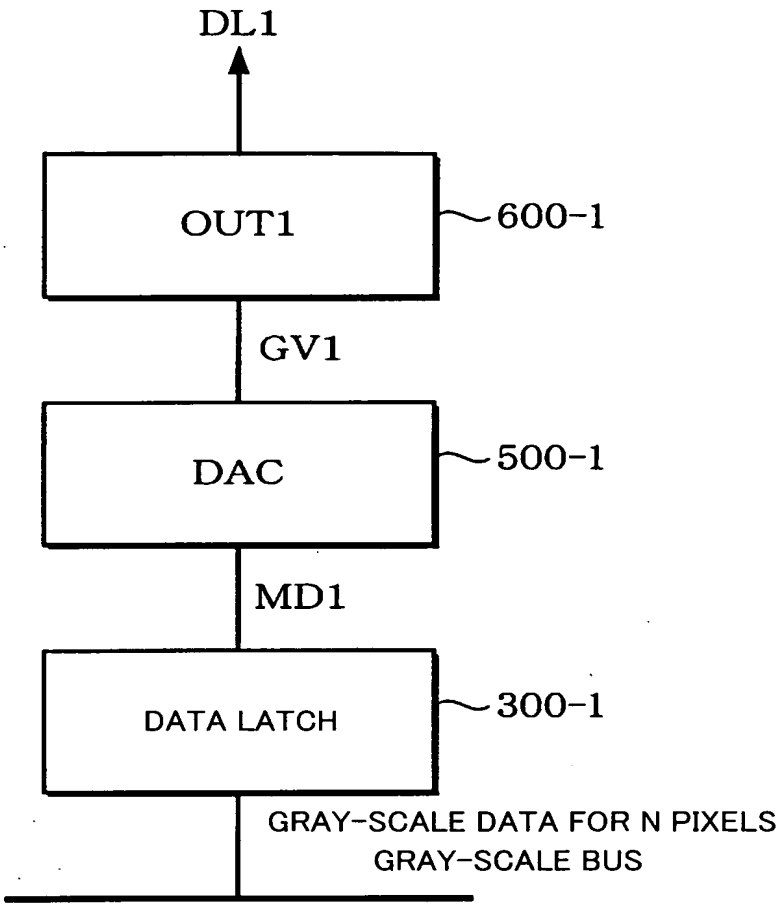

DL1
OUT1
600-1
GV1
DAC
500-1
MD1
DATA LATCH
300-1
GRAY-SCALE DATA FOR N PIXELS
GRAY-SCALE BUS

FIG. 14

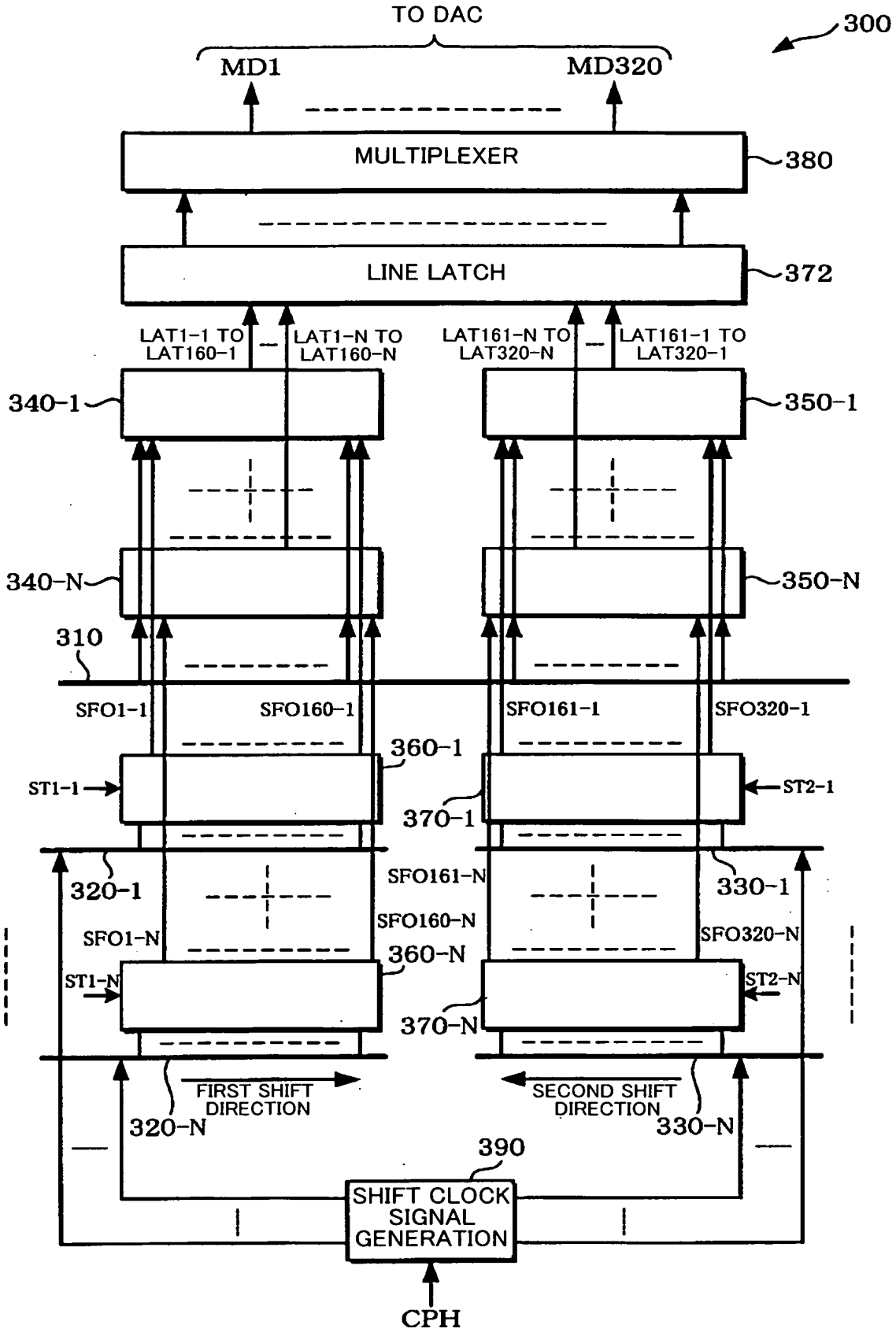

TO DAC
300
MD1
MD320
MULTIPLEXER
380
LINE LATCH
372
LAT1-1 TO LAT160-1
LAT1-N TO LAT160-N
LAT161-N TO LAT320-N
LAT161-1 TO LAT320-1
340-1
350-1
340-N
350-N
310
SFO1-1
SFO160-1
SFO161-1
SFO320-1
360-1
370-1
ST1-1
ST2-1
320-1
SFO161-N
330-1
SFO1-N
SFO160-N
SFO320-N
360-N
ST1-N
ST2-N
370-N
FIRST SHIFT DIRECTION
SECOND SHIFT DIRECTION
320-N
330-N
390
SHIFT CLOCK SIGNAL GENERATION
CPH

FIG. 15

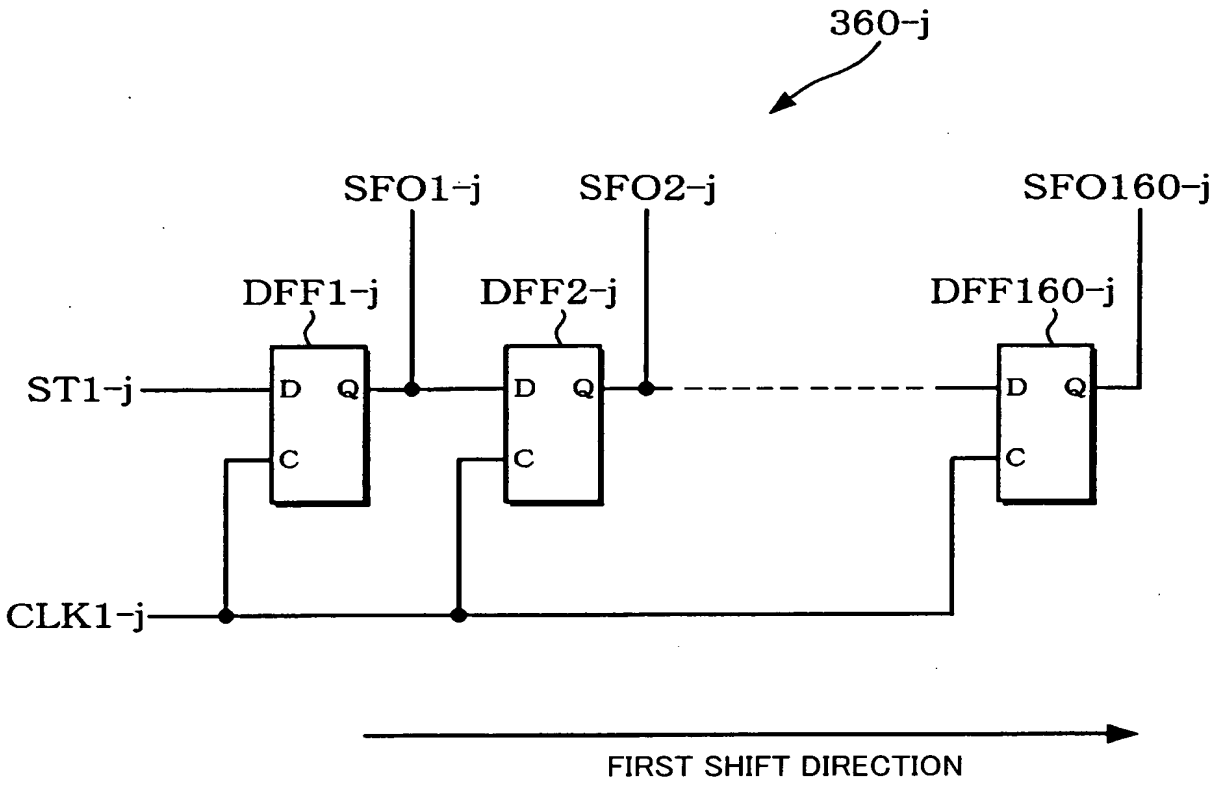

360-j
SFO1-j
SFO2-j
SFO160-j
DFF1-j
DFF2-j
DFF160-j
ST1-j
D
Q
C
CLK1-j
FIRST SHIFT DIRECTION

FIG. 16

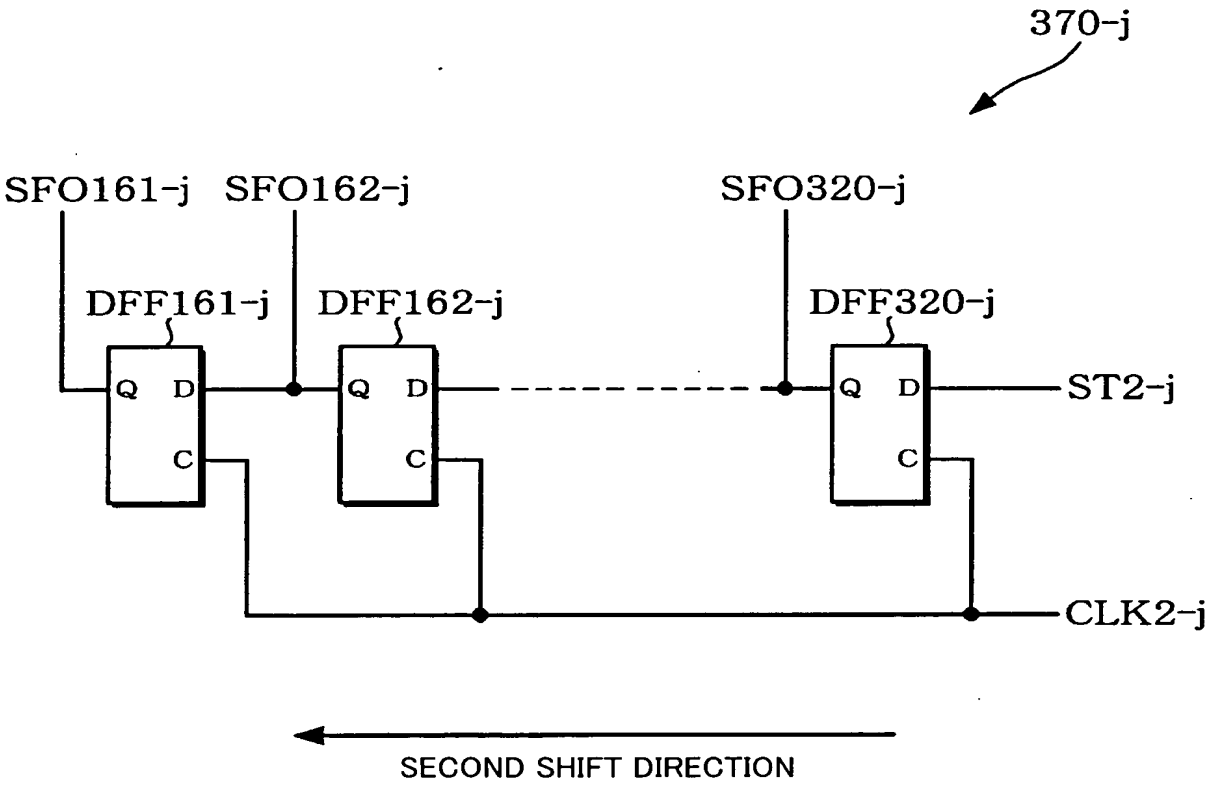

370-j
SFO161-j
SFO162-j
SFO320-j
DFF161-j
DFF162-j
DFF320-j
Q
D
C
ST2-j
CLK2-j
SECOND SHIFT DIRECTION

FIG. 17

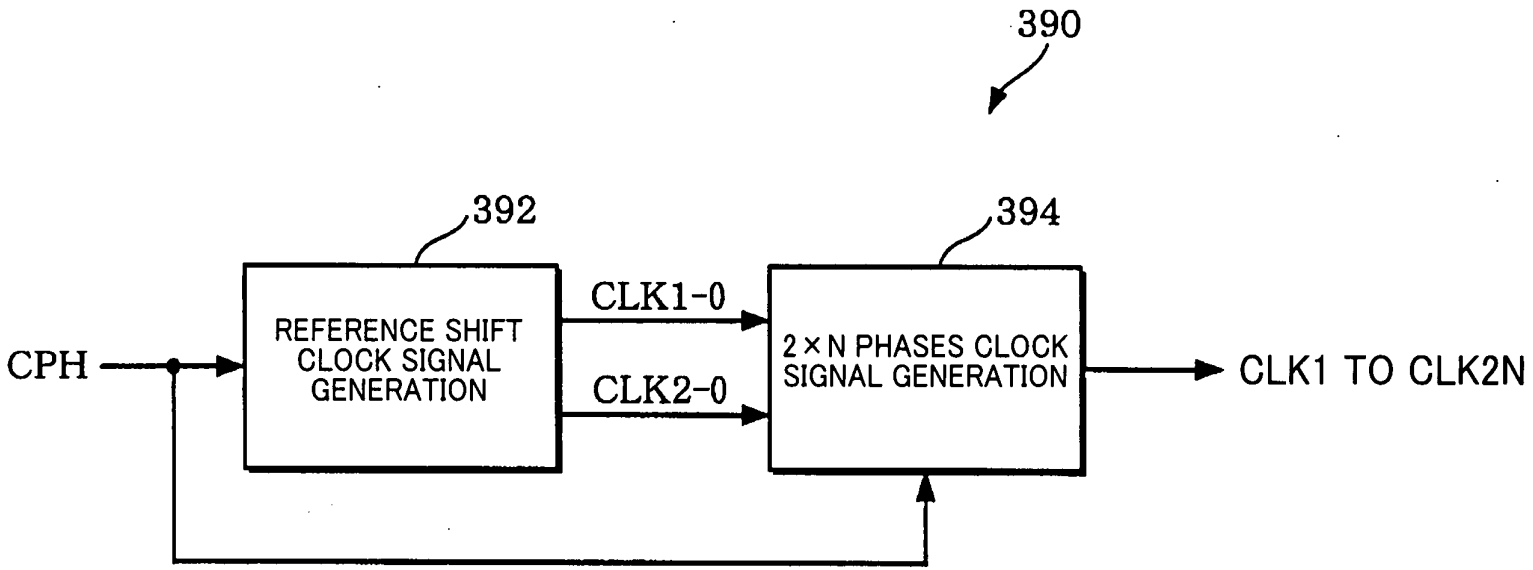
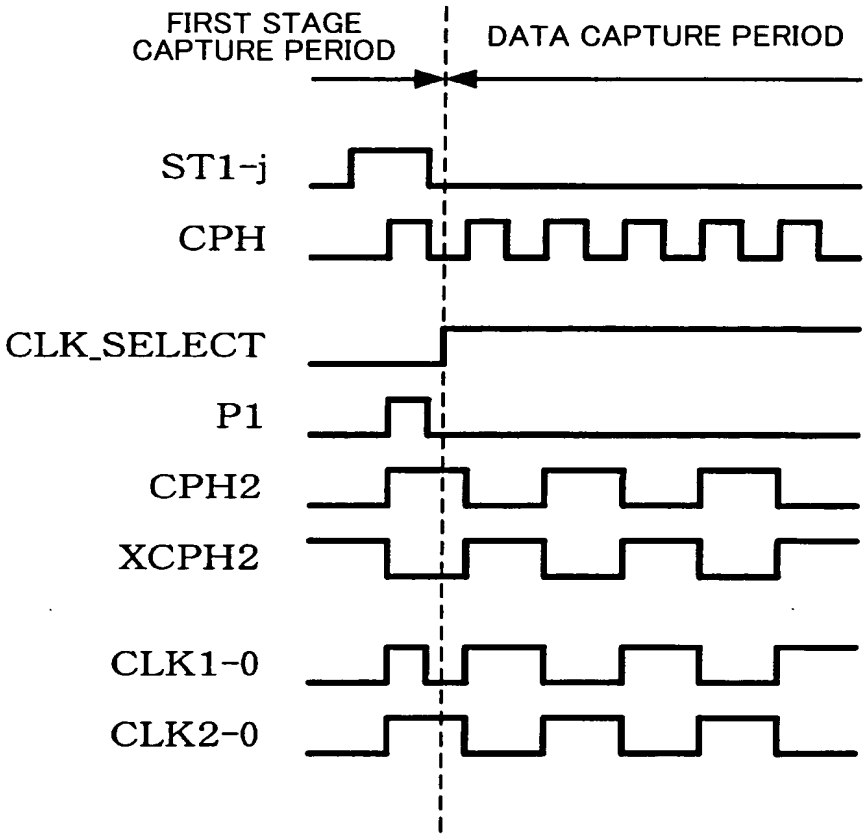

390
392
394
CPH
REFERENCE SHIFT CLOCK SIGNAL GENERATION
CLK1-0
CLK2-0
2×N PHASES CLOCK SIGNAL GENERATION
CLK1 TO CLK2N

FIG. 18


FIRST STAGE CAPTURE PERIOD
DATA CAPTURE PERIOD
ST1-j
CPH
CLK_SELECT
P1
CPH2
XCPH2
CLK1-0
CLK2-0

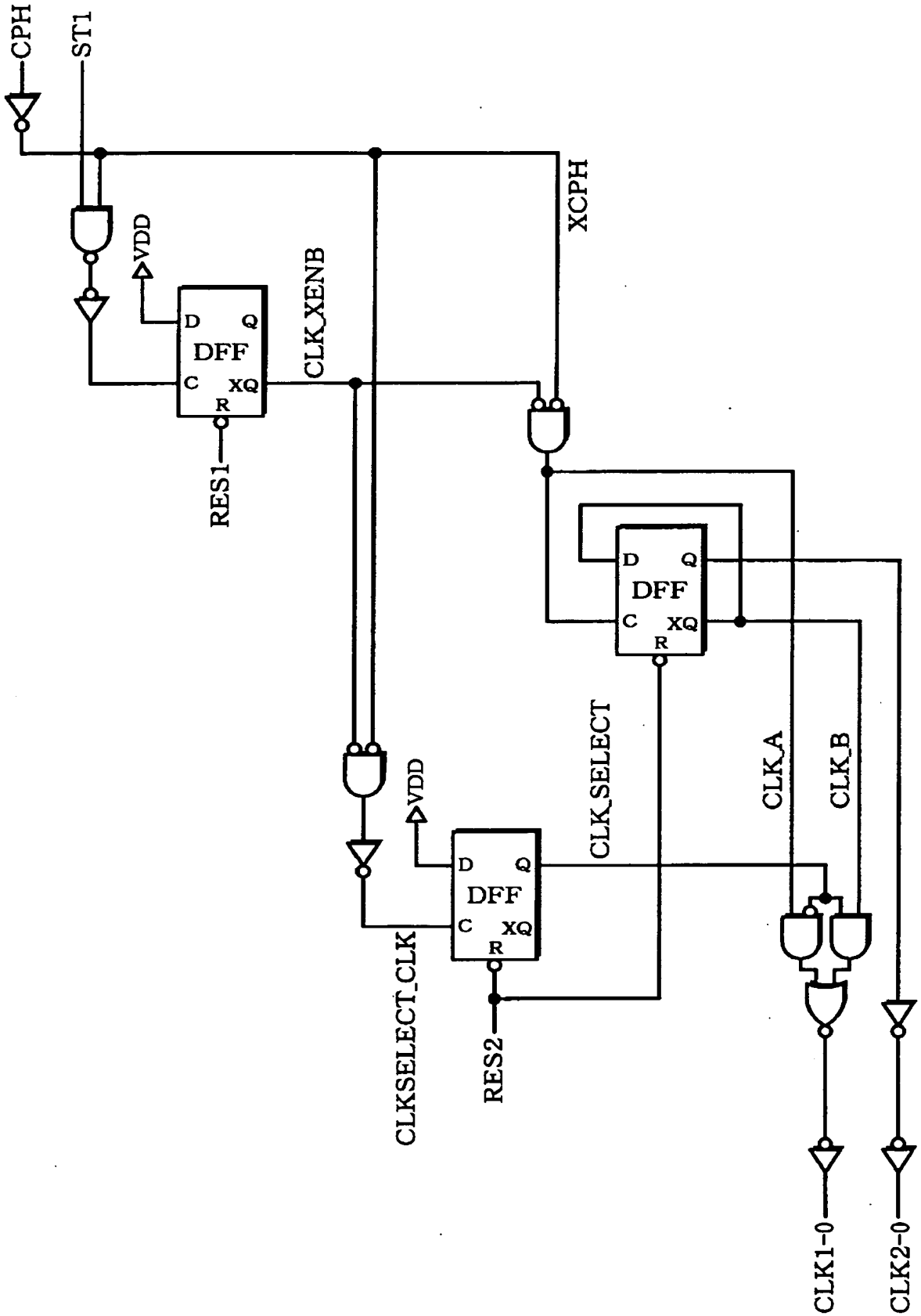

CPH
ST1
VDD
DFF
D
Q
C
XQ
R
RES1
CLK_XENB
XCPH
DFF
D
Q
C
XQ
R
CLK_SELECT
CLK_A
CLK_B
VDD
DFF
D
Q
C
XQ
R
CLKSELECT_CLK
RES2
CLK1-0
CLK2-0

FIG. 19

FIG. 20

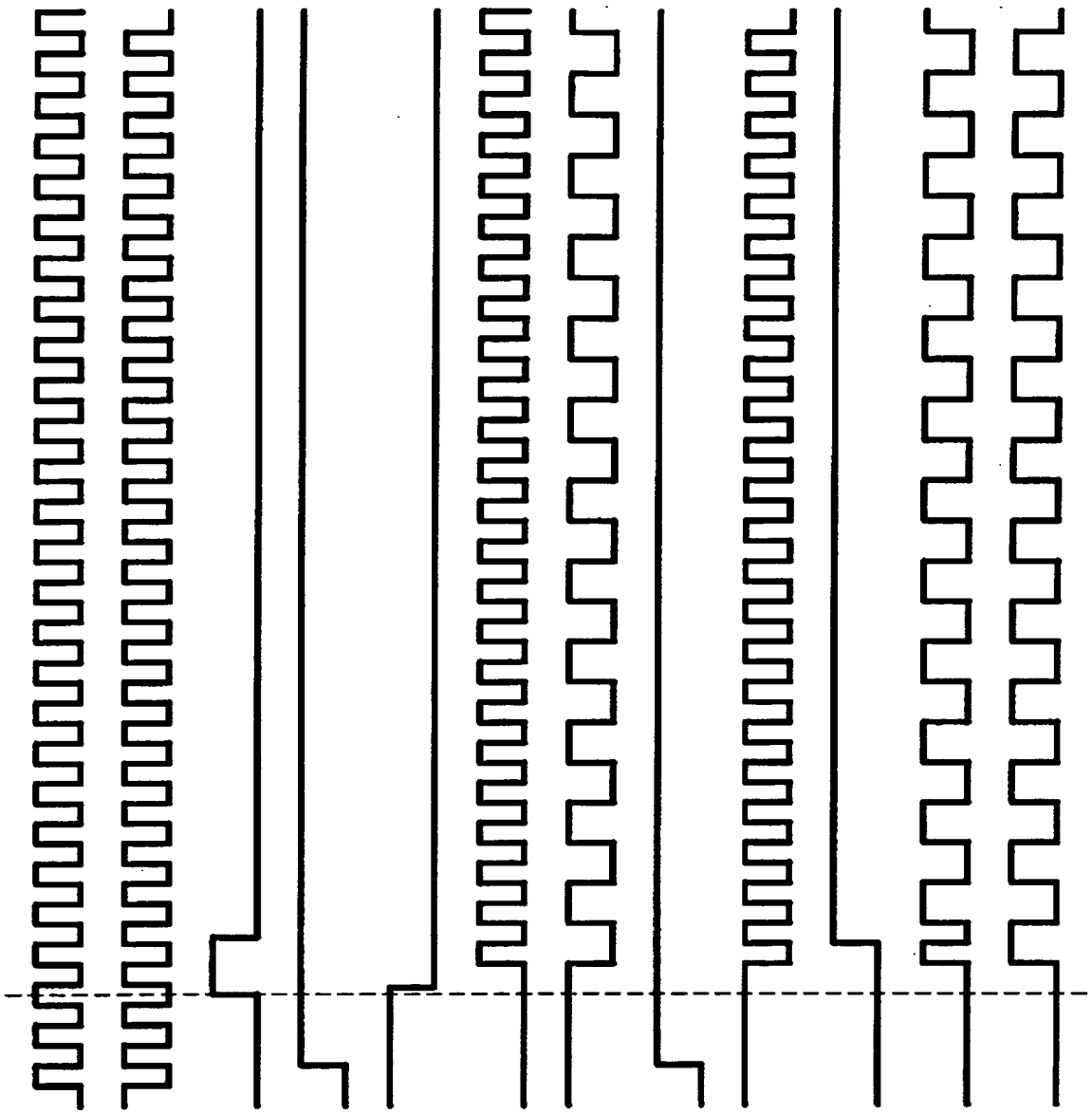

CPH
XCPH
ST1
RES1
CLK_XENB
CLK_A
CLK_B
RES2
CLKSELECT_CLK
CLK_SELECT
CLK1-0
CLK2-0

FIG. 21

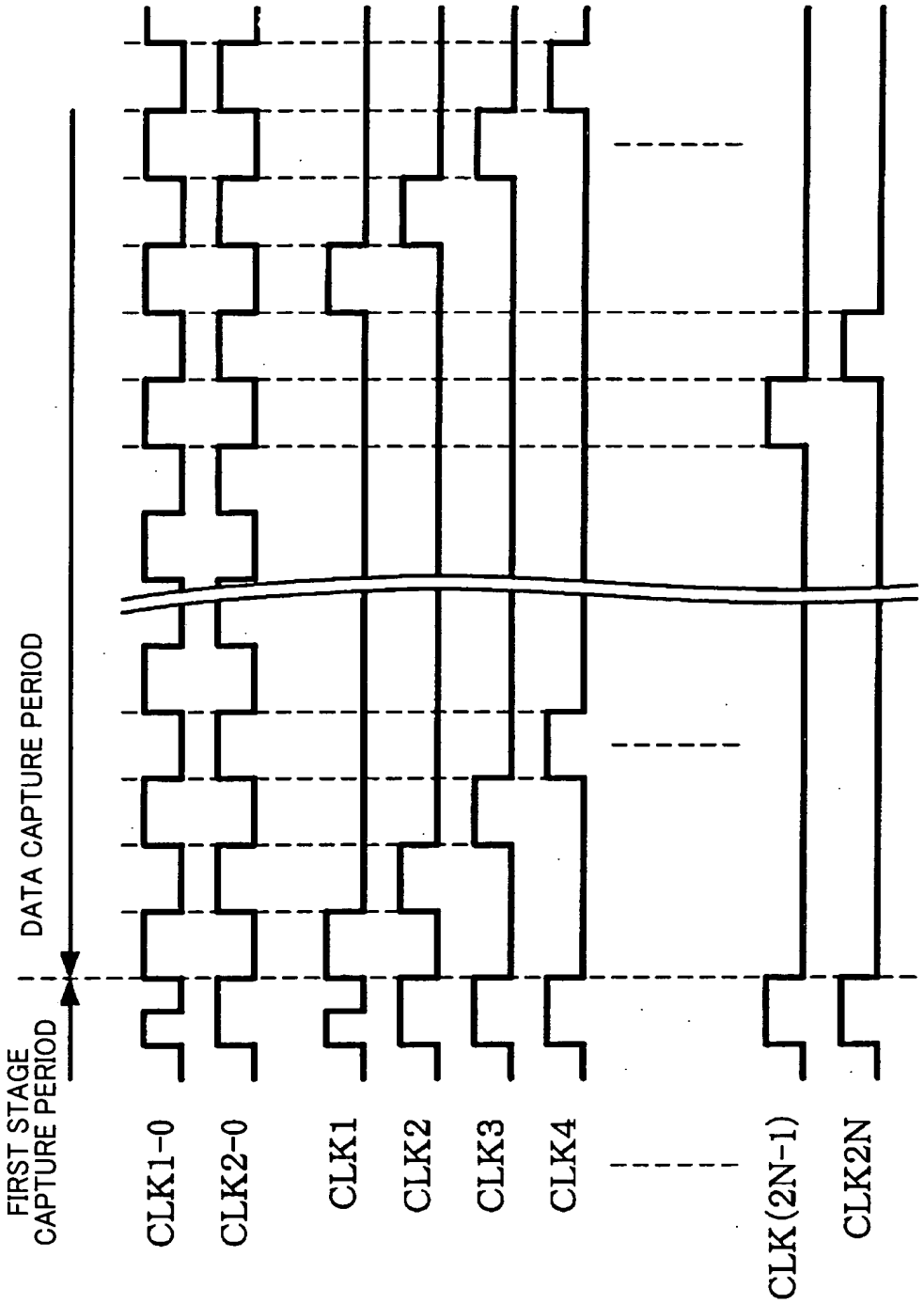

FIRST STAGE CAPTURE PERIOD
DATA CAPTURE PERIOD
CLK1-0
CLK2-0
CLK1
CLK2
CLK3
CLK4
CLK(2N-1)
CLK2N

FIG. 22

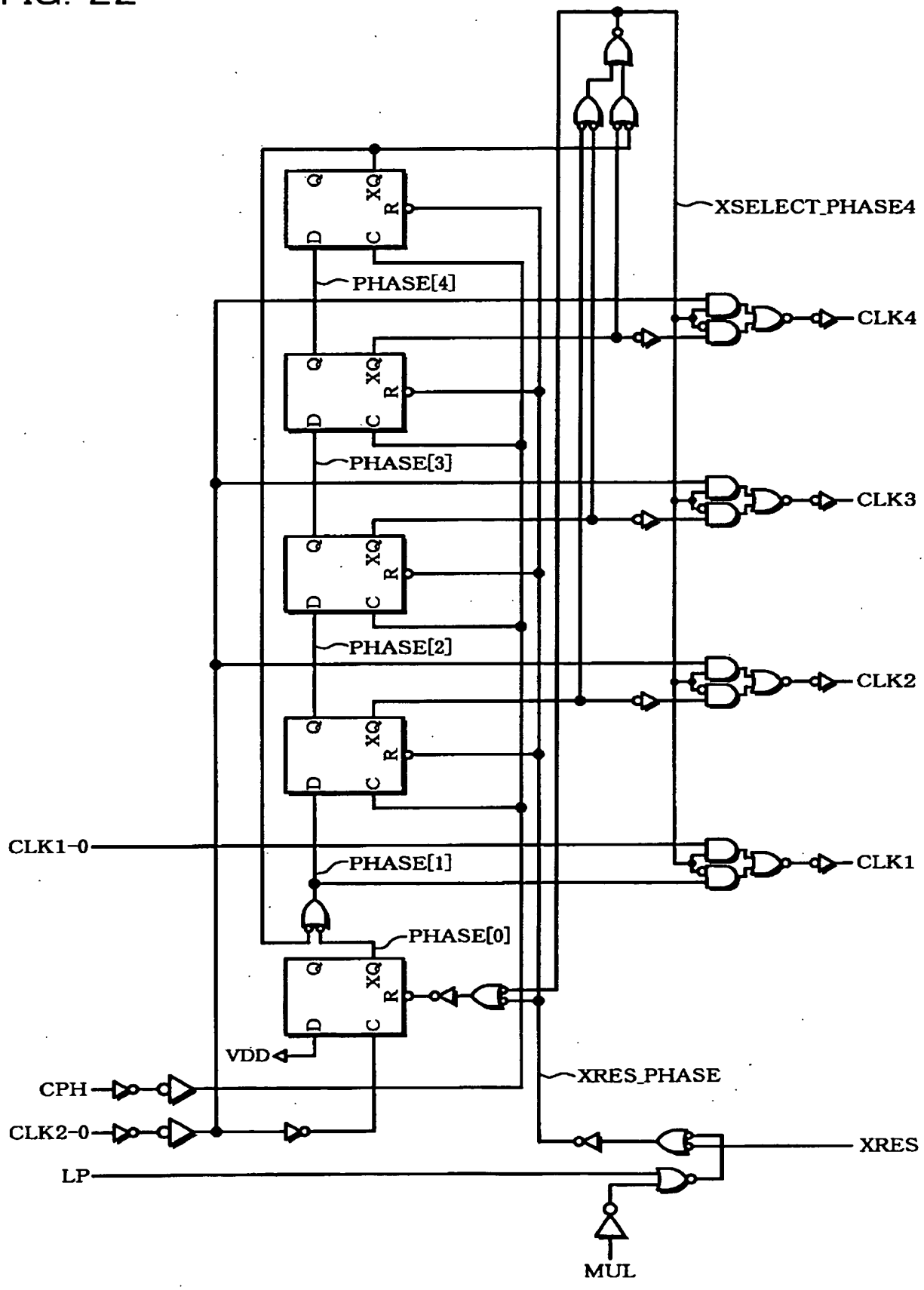

XSELECT_PHASE4
PHASE[4]
CLK4
PHASE[3]
CLK3
PHASE[2]
CLK2
CLK1-0
PHASE[1]
CLK1
PHASE[0]
VDD
CPH
XRES_PHASE
CLK2-0
XRES
LP
MUL
Q
XQ
R
D
C

FIG. 23

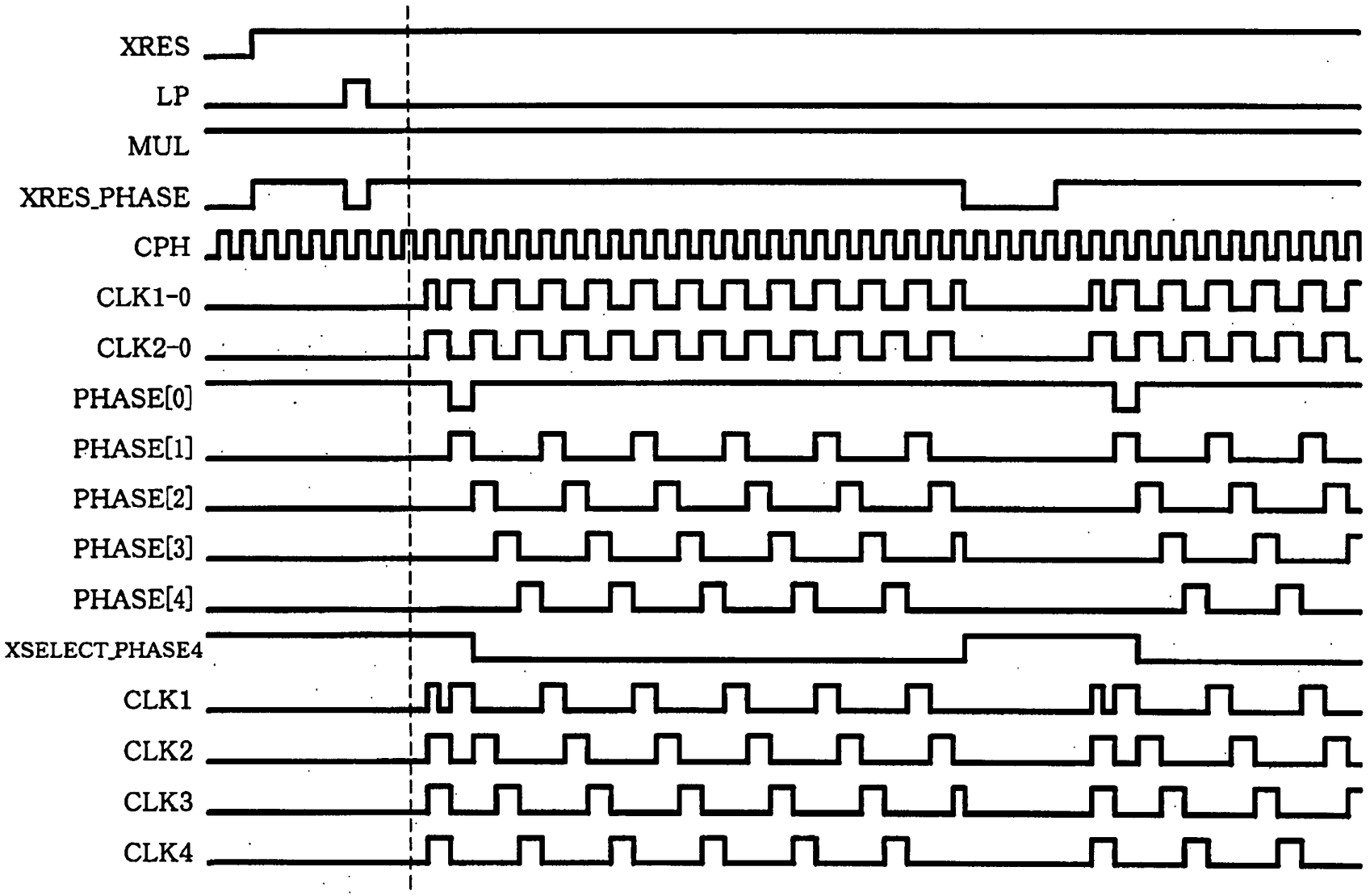

XRES
LP
MUL
XRES_PHASE
CPH
CLK1-0
CLK2-0
PHASE[0]
PHASE[1]
PHASE[2]
PHASE[3]
PHASE[4]
XSELECT_PHASE4
CLK1
CLK2
CLK3
CLK4

FIG. 24

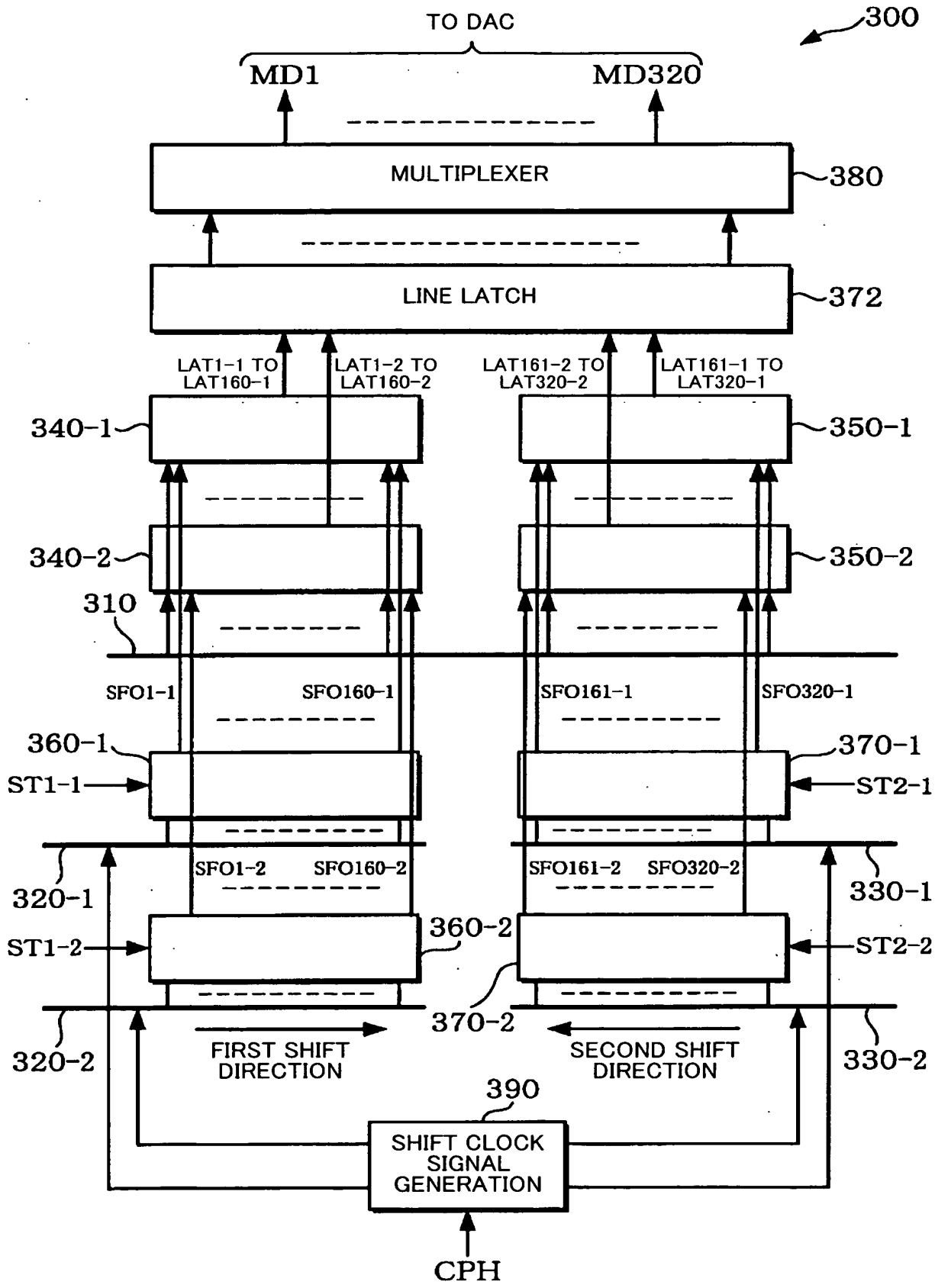

TO DAC
300
MD1
MD320
MULTIPLEXER
380
LINE LATCH
372
LAT1-1 TO LAT160-1
LAT1-2 TO LAT160-2
LAT161-2 TO LAT320-2
LAT161-1 TO LAT320-1
340-1
350-1
340-2
350-2
310
SFO1-1
SFO160-1
SFO161-1
SFO320-1
360-1
370-1
ST1-1
ST2-1
SFO1-2
SFO160-2
SFO161-2
SFO320-2
320-1
330-1
ST1-2
360-2
ST2-2
370-2
320-2
330-2
FIRST SHIFT DIRECTION
SECOND SHIFT DIRECTION
390
SHIFT CLOCK SIGNAL GENERATION
CPH

FIG. 25

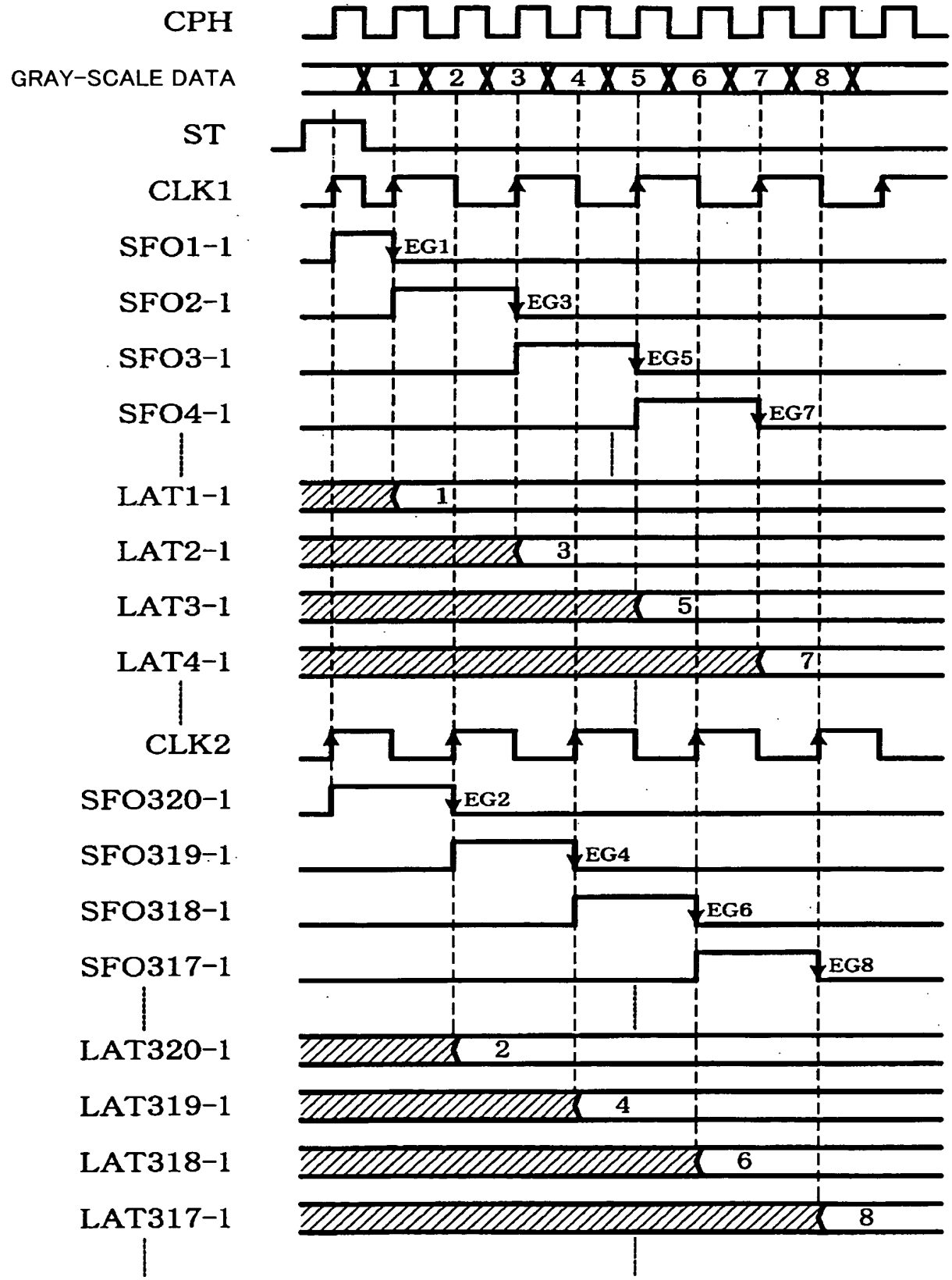
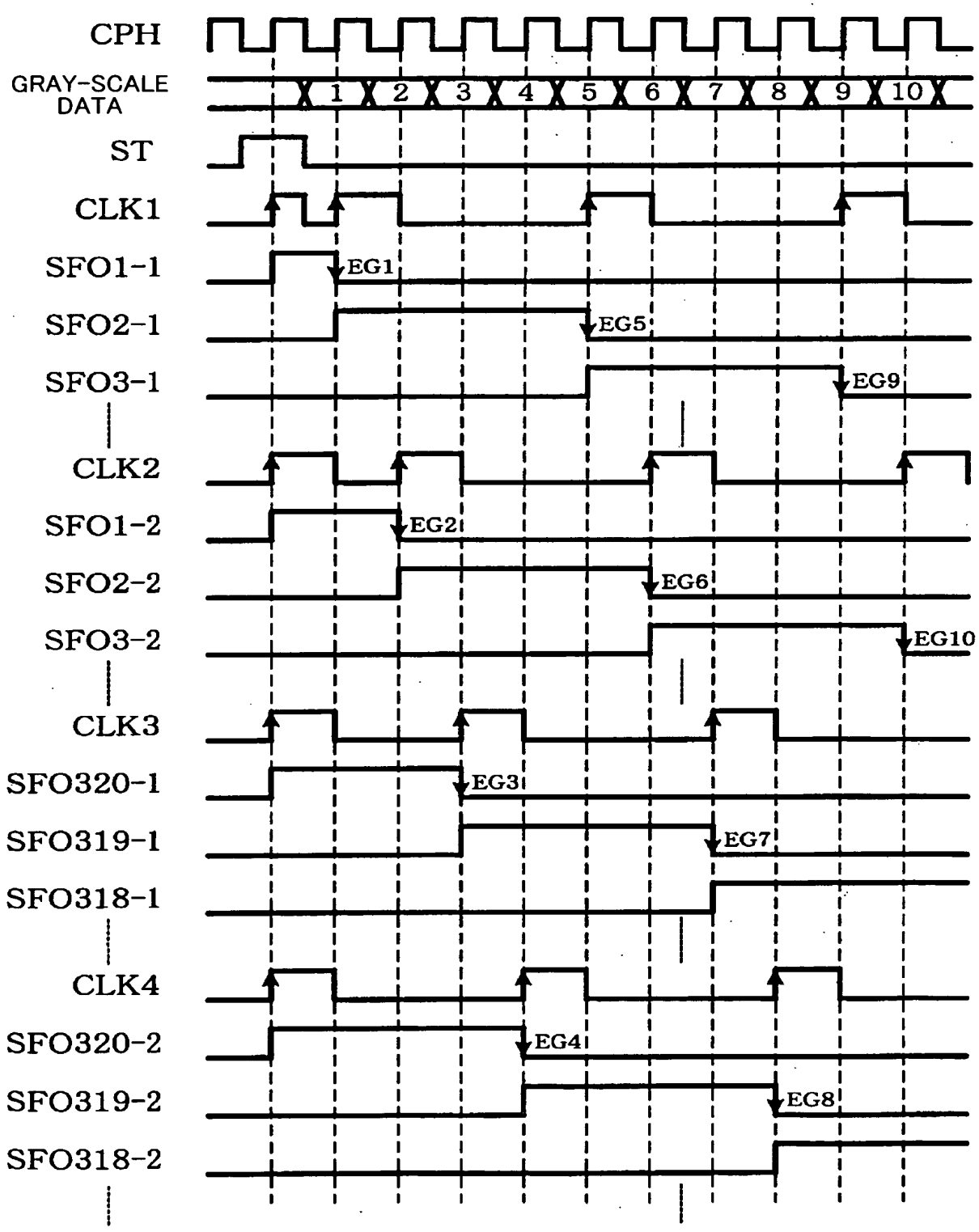

CPH
GRAY-SCALE DATA
1
2
3
4
5
6
7
8
ST
CLK1
SFO1-1
EG1
SFO2-1
EG3
SFO3-1
EG5
SFO4-1
EG7
LAT1-1
1
LAT2-1
3
LAT3-1
5
LAT4-1
7
CLK2
SFO320-1
EG2
SFO319-1
EG4
SFO318-1
EG6
SFO317-1
EG8
LAT320-1
2
LAT319-1
4
LAT318-1
6
LAT317-1
8

FIG. 26


CPH
GRAY-SCALE DATA
1
2
3
4
5
6
7
8
9
10
ST
CLK1
SFO1-1
EG1
SFO2-1
EG5
SFO3-1
EG9
CLK2
SFO1-2
EG2
SFO2-2
EG6
SFO3-2
EG10
CLK3
SFO320-1
EG3
SFO319-1
EG7
SFO318-1
CLK4
SFO320-2
EG4
SFO319-2
EG8
SFO318-2